REMARKS

This communication responds to the Office Action mailed on February 3, 2005. No claims are amended, no claims are canceled, and no claims are added. As a result, claims 7-26 are now pending in this Application. The claims are reproduced in Appendix A for convenient reference by the Examiner.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned Application is the Assignee, Intel Corporation.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences or appeals known to Appellant, Appellant's legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in an appeal in this matter.

3. STATUS OF THE CLAIMS

Claims 7-26 are currently pending in the Application. Claims 7-26 stand rejected, and the rejection is appealed herein.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the amendments to claims 7 and 14-15 to correct typographical errors in conjunction with a Response to Restriction Requirement mailed on September 15, 2004. New claims 17-26 were also added in this Response.

5. SUMMARY OF CLAIMED SUBJECT MATTER

This summary is presented in compliance with the requirements of Title 37 C.F.R. § 41.37(c)(1)(v), mandating a "concise explanation of the subject matter defined in each of the independent claims involved in the appeal ...". Nothing contained in this summary is intended

to change the specific language of the claims described, nor is the language of this summary to be construed so as to limit the scope of the claims in any way.

Some embodiments of the invention are related to an integrated circuit including a phase lock loop. The phase lock loop may include a voltage-to-current circuit to influence a voltage on a capacitor, a voltage controlled oscillator (responsive to the voltage on the capacitor) to provide a second clock signal, and a sampling circuit responsive to a first clock signal and the second clock signal. The sampling circuit may generate two voltage values. The difference of the two voltage values may be a function of the phase difference between the first and second clock signals. (Application: Claim 7; FIGs. 1-3, and 7; and paragraphs 9-18, 30-32)

Some embodiments of the invention are related to an integrated circuit including a phase lock loop having a voltage-to-current circuit to influence a voltage on a capacitor, a voltage controlled oscillator responsive to the voltage on the capacitor to provide a second clock signal, and a sampling circuit responsive to a first clock signal and the second clock signal. The sampling circuit may generate two voltage values, such that the difference of the two voltage values is a function of the phase difference between the first and second clock signals. The integrated circuit may also include a plurality of sequential elements coupled to the phase lock loop. (Application: Claim 12; FIGs. 2, 5, and 7; and paragraphs 30-32)

Some embodiments of the invention are related to a phase lock loop including a voltage controlled oscillator to generate a differential signal on two nodes, and a phase detector to compare the phase of the differential signal and the phase of a received signal. The phase detector may include a sampling circuit to periodically sample voltage values on the two nodes, and a linear voltage-to-current converter responsive to the voltage values to create a control voltage for the voltage controlled oscillator. (Application: Claim 17; FIGs. 1-3; and paragraphs 9-18)

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

6.1 Claims 7-11 and 17-26 stand rejected under 35 USC § 103(a) as being unpatentable over Soyuer (U.S. 5,422,603; hereinafter "Soyuer") in view of Matsui (U.S. 6,300,803; hereinafter "Matsui").

6.2 Claims 12-16 stand rejected under 35 USC § 103(a) as being unpatentable over Ishikawa (U.S. 5,748,018; hereinafter "Ishikawa") in view of Soyuer and Matsui.

7. ARGUMENT

7.1 The Applicable Law

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). References must be considered in their entirety, including parts that teach away from the claims. See MPEP § 2141.02.

The Examiner must avoid hindsight. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)). That is, the Examiner cannot use the Appellant's structure as a "template" and simply select elements from the references to reconstruct the claimed invention. *In re Gorman*, 933 F.2d 982, 987, 18 U.S.P.Q.2d (BNA) 1885, 1888 (Fed. Cir. 1991). If the proposed modification renders the prior art invention being modified

unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)).

7.2 The References

Soyeur: discloses a CMOS synthesizer including a phase frequency detector (PFD) 300 coupled to a voltage controlled oscillator (VCO) 100 having two control inputs. See Soyuer, FIG. 1 and Col. 2, lines 20-30. The architecture of the design is fully symmetric, so as to minimize cross-over distortion in the region of zero phase difference commonly found when using asymmetric configurations. See Soyuer, Col. 1, lines 9-17; and Col. 4, lines 10-12.

Matsui: teaches a phase-comparison circuit that operates by converting two voltage signals Vin1 and Vin2 at the input into a single output, current Iout, representing the difference in phase between the two input voltages. See Matsui, FIG. 8; Col. 1, lines 5-8; and Col. 7, lines 3-8 and 39-58.

Ishikawa: describes a data transfer system having a shortened data transfer cycle. The shortened cycle is achieved by delaying both the clock and data input signals by a selected amount so that the clock and data signals may be provided closer together. It is specifically noted that phase-locked loops are to be avoided in the invention, as they provide the undesirable attributes of momentary instability and increased die area. See Ishikawa, FIGs. 1C-1D and 3A-3B; Col. 2, lines 1-13 and 23-27; and Col. 4, line 34 – Col. 5 line 28.

7.3 Discussion of the Rejections

7.3.1 The Rejections Under § 103:

Claims 7-11 and 17-26 stand rejected under 35 USC § 103(a) as being unpatentable over Soyuer in view of Matsui. Claims 12-16 stand rejected under 35 USC § 103(a) as being unpatentable over Ishikawa in view of Soyuer and Matsui. First, the Appellant does not admit

that Soyeur, Matsui, or Ishikawa are prior art, and reserves the right to swear behind these references in the future. Second, since a *prima facia* case of obviousness has not been established in each case, the Appellant respectfully traverses this rejection.

No proper *prima facie* case of obviousness has been established in this case because (1) there is no motivation to combine the references, (2) there is no reasonable expectation of success if the references are combined, and (3) no combination of the references discloses all the limitations set forth in the claims. Each of these points will be explained in detail, as follows.

There Is No Motivation to Combine the References. With respect to claims 7-11 and 17-26, it is asserted in the Office Action that "it would have been obvious ... to use the specific [phase-comparison] circuit of Matsui for the broad phase detector 300 of Soyuer for the expected advantage of offset compensation." It is also alleged that "Soyuer fails to disclose any specific details for the broad phase detector 300." However, Soyuer does teach several elements required by the VCO 100 (and provided by the broad phase detector 300) for proper operation. These elements are not (and can not be) provided by the phase-comparison circuit of Matsui.

The VCO 100 of Soyuer is controlled using two separate output signals derived from the PFD 300. Soyuer, Col. 2, lines 28-32. As can be seen in FIG. 2 of Soyuer, the PFD 300 is a fully symmetric PFD. It is the "fully symmetric architecture ... [that] minimizes the effect of the dead-zone on PFD performance." See Soyuer, Col. 4, lines 9-12. According to Soyuer, "the UP or DN outputs and their complements, UPB or DNB .... [have] duty cycles [that] are proportional to the phase and frequency difference between the inputs R/RB and V/VB." Soyuer, Col. 3, lines 61-64. Thus, the PFD 300 of Soyuer provides two outputs to the VCO 100: one for the difference in phase (similar to Iout of Matsui), and the other *for the difference in frequency*. The VCO 100 requires *both* of these control signals, processed through parallel delay lines of different lengths, to function properly. Soyuer, Col. 2, lines 28-43. In other words, if the VCO 100 of Soyuer does not receive both *phase and frequency* control inputs (e.g., as supplied by Soyuer's PFD 300), it will not operate. Matsui does not provide the needed frequency difference output.

To modify Soyuer to use the phase-comparison circuit of Matsui renders Soyuer inoperable, since this combination would attempt to control a dual-input phase/frequency VCO

(Soyuer) using the single, phase-only output provided by Matsui. The single output (Iout) of Matsui's phase-comparison circuit is not symmetric, and would not allow the charge-pump filter of Soyuer to provide a differential output, which is "exactly what is required to reduce the susceptibility of the charge pump to crossover distortion for small phase differences between the PFD input signals." See Soyuer, Col. 5, 38-41. Since modifying the VCO of Soyuer to make use of Matsui's phase-comparison circuit (that provides no frequency difference information) would render Soyuer's device inoperable, there is no motivation to combine these references.

With respect to the rejection of claims 12-16, the Office also relies on the assumption of fundamental compatibility between Soyuer's VCO 100 and Matsui's phase comparison circuit. However, as noted previously, the suggested combination is not operable. The addition of Ishikawa's phase lock loop 613 and elements 100, 200 does nothing to remedy the non-compatible combination of Soyuer and Matsui.

Further, there is no evidence in the record to support the assertion by the Office that "it would have been obvious to use the specific PLL in the above combination to Soyner [sic] and Matsui for the broad PLL 613 in the reference to Ishikawa to obtain the expected advantage of offset compensation therein." The asserted advantage of "offset compensation" offered in the Office Action is not noted as desirable by Soyuer or Ishikawa. In fact, Ishikawa specifically teaches away from the use of any kind of PLL, stating "[a]nother object of the present invention is to provide a data transfer system ... without using the PLL circuit which makes the device unstable because of the lock time and which results in increase chip area." Ishikawa, Col. 2, lines 22-27. This use of a contradictory and unsupported assertion does not satisfy the explicit requirements set forth by the *In re Sang Su Lee* court. *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002) (motivation must be supported by evidence in the record). Thus, the Examiner appears to be using personal knowledge, and is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2). Thus, there is no motivation to combine Soyeur, Matsui, and Ishikawa.

There Is No Reasonable Expectation of Success. Combining Soyuer and Matsui does not achieve or advance the goals of either system. Adding the phase-comparison circuit of Matsui (providing a single, phase-only output) to Soyuer's dual-input phase/frequency VCO

takes away the advantage of Soyuer's design to minimize "the high-speed mismatch effects from the switching speeds and bias currents of NMOS and PMOS devices." See Soyuer, Col. 5, lines 34-38.

Similarly, Matsui is directed to providing a current mirror within a phase-comparison circuit to compensate for errors between a reference current and an output current. See Matsui, Col. 3, lines 39-44. The circuitry of Soyuer, dealing with differential voltages, does nothing to assist in this endeavor. Thus, combining Soyuer and Matsui does not convey a reasonable expectation of success in either case.

As noted previously, the rejection of claims 12-16 relies on the fundamental assumption of inter-operability between Soyuer's VCO 100 and Matsui's phase comparison circuit. However, this combination is not compatible, and the addition of Ishikawa's phase lock loop 613 and elements 100, 200 does nothing to transform the combination of Soyuer and Matsui into an apparatus capable of successful operation. In fact, the combination suggested by the Office is specifically addressed by Ishikawa as one that is to be avoided. It is respectfully noted that the fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01.

The References Do Not Teach All Claim Limitations. The PFD 300 of Soyuer does not include a "voltage-to-current circuit to influence a voltage on a capacitor" and a "voltage controlled oscillator responsive to the voltage on the capacitor" as claimed by the Applicants in independent claims 7 and 12 (and in dependent claims 8-11, 13-16, and 23-26). Nor does Soyuer include a "voltage controlled oscillator to generate a differential signal on two nodes", a "sampling circuit to periodically sample voltage values on the two nodes" and a "linear voltage-to-current converter responsive to the voltage values to create a control voltage for the voltage controlled oscillator" as claimed by the Applicants in independent claim 17 (and in dependent claims 18-22).

In addition, niether Matsui nor Ishikawa discloses a "voltage-to-current circuit to influence a voltage on a capacitor" and a "voltage controlled oscillator responsive to the voltage

on the capacitor" as claimed by the Applicants in 12 (and in dependent claims 13-16). In fact, Matsui's phase comparison circuit is current-based.

The Office attempts to attribute the combination of Soyuer and Matsui with the attributes of "voltage-to-current circuit to influence a voltage on a capacitor" and a "voltage controlled oscillator responsive to the voltage on the capacitor". However, this combination, as explained above, is inoperative. Thus, no combination of Soyuer, Matsui, or Ishikawa can provide these missing elements.

Therefore, a *prima facie* case of obviousness has not been established by the combination of Soyuer, Matsui, or Ishikawa. There is no motivation to combine the references (in fact, the references teach away from such a combination), there is no reasonable expectation of success if the references are combined, and any combination of the references would not teach all of the limitations in the claims. Therefore, it is respectfully asserted that no proper combination of Soyuer, Matsui, or Ishikawa can be made to disclose the embodiments claimed, and it is respectfully requested that the rejection of claims 7-26 under 35 U.S.C. §103 be reconsidered and withdrawn.

8. SUMMARY

It is respectfully submitted that no *prima facie* case of obviousness under 35 U.S.C. §103 has been established by the Office. Therefore, it is respectfully requested that the rejection of claims 7-26 be reconsidered and withdrawn. The Appellant respectfully submits that all of the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Appellant's attorney, Mark Muller at (210) 308-5677, or the undersigned attorney at (612) 349-9592, to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 4th day of April 2005.

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